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10/587,596	04/24/2007	Wolfgang Schnitt	DE04 0034 US1	2386

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EXAMINER	
HUBER, ROBERT T	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
09/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/587,596	SCHNITT ET AL.	
	Examiner	Art Unit	
	ROBERT HUBER	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on June 11, 2008. These drawings are accepted.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Momodomi et al. (US 4,881,113).

a. Regarding claim 1, Momodomi discloses **an integrated circuit chip** (e.g. figures 2a and 2b), **comprising in sequence,**

a substrate layer of a substrate material (substrate 11),

an insulating layer of an insulating material (region 13),

a first electrically conductive layer of a first electrically conductive material (electrode 17, as disclosed in col. 3, lines 1 – 2),

a dielectric layer of a dielectric material (Silicon Oxide layers 14 and 20, which is also between the electrodes 17 and 18, as discussed in col. 2, line 66 and col. 3, lines 4 – 9) and

a second electrically conductive layer of a second electrically conductive material (electrode 18),

said IC chip comprising at least one integrated circuit and at least one integrated electrostatic discharge protection device (as disclosed in col. 1, lines 46 – 48), **said electrostatic discharge protection device comprising,**

a pair of spaced center and circumferential electrodes (electrodes 17 and 18, as seen in figure 2b)**, the center electrode being formed by the first electrically conductive layer and the circumferential electrode being formed by the second electrically conductive layer** (as discussed in col. 3, lines 1 - 2), **said electrodes being separated by a toroidal spark gap cavity** (ring shaped region between electrodes 17 and 18 filled with Silicon Oxide, as discussed in col. 3, lines 4 – 7, and clarified in the figure below), **wherein the toroid of the toroidal spark gap cavity comprises,**

a base layer formed by the insulating layer of the integrated circuit chip (layer 13, as seen in figure 2b),

a side wall formed by the circumferential electrode (e.g. as seen in figure 2b),

a cover layer formed by the dielectric layer of the integrated circuit chip (e.g. as seen in figure 2b, layer 20 covers the spark gap cavity), **and the center of the toroid being formed by the center electrode comprising a contact pad in contact with the insulating layer** (e.g. as seen in figure 2b),

said electrostatic discharge protection device also comprising means to electrically connect the center electrode to input circuit paths to be protected from electrostatic discharge (e.g. figure 2a, electrode 25, as

disclosed in col. 3, lines 12 – 14) **and means to electrically connect the circumferential electrode to an electrostatic discharge path comprising either a connection to a circuit ground or a circuit supply voltage** (e.g. figure 2a, electrode 19, as disclosed in col. 3, lines 5 – 7).

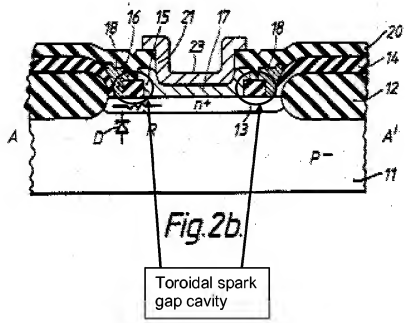

Fig.2b.

b. Regarding claim 2, **Momodomi discloses the integrated circuit chip of claim 1, as cited above, further comprising a passive component selected from the group comprising resistors, capacitors, and inductors** (e.g. figures 4a and 4b show the equivalent circuit of figures 2a and 2b, as discloses in col. 4, lines 12 - 16, which shows a resistor in the circuit).

c. Regarding claim 4, **Momodomi discloses the integrated circuit chip of claim 1, as cited above, wherein the second electrically conductive material**

is aluminum (col. 3, lines 1 – 2 disclose the second electrode 18 to be aluminum Al. Col. 6, lines 30 – 32 also disclose that it may be made from Mo and W instead of Al).

d. Regarding claim 6, **Momodomi discloses the integrated circuit chip of claim 1, as cited above, wherein the substrate material is selected from the group comprising silicon, glass and a ceramic material** (col. 2, line 64 discloses the substrate to be made of silicon).

4. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by El-Kareh et al. (US 5,933,718). **El-Kareh discloses a method of fabricating an integrated circuit chip comprising an integrated circuit and an electrostatic discharge protection device** (e.g. see figures 1A - 1E and 2) **comprising the steps of**

a) **providing a semiconductor substrate** (substrate 10),

b) **depositing an insulating layer on semiconductor substrate** (gate oxide 151 col. 1, line 56),

c) **depositing a first electrically conductive layer of a first electrically conductive material on said insulating layer** (polysilicon layer 152, col. 1, line 56),

d**) depositing a dielectric layer of a dielectric material on said first electrically conductive layer** (dielectric layer 156 of silicon nitride, col. 1, line 58),

e) **etching spaced contact windows for a center electrode** (etched window 100, shown in figure 1B, as discussed in col. 2, lines 25 - 26) **and a circumferential electrode** (window 211 of figure 1D, as discussed in col. 2, lines 59 - 63),

f) **depositing a mask** (e.g. col. 2, lines 32 – 35 discuss the conventional use of blocking parts of the device with photoresist, which is a mask, and col. 2, lines 1 -2, discuss the use of photoresist to selectively remove materials),

g) **etching a hollow groove into the first electrically conductive layer under the circumference of the contact window of the circumferential electrode** (e.g. figure 1B shows groove 112 formed into the first conducting layer 152, which is formed by etching, as discussed in col. 2, lines 26 – 50),

h) **depositing a layer of a second electrically conductive layer** (e.g. figure 2, layer 170 and 178, which is formed simultaneously, as discussed in col. 3, lines 26 – 27, and are made of a conductor, as discussed in col. 2, line 67 through col. 3 line 2) **through the contact window of the center electrode to mechanically contact the insulating layer** (e.g. figure 2 shows the conducting layer 170 in mechanical contact to the oxide layer 151, via the oxide layer 153. Layer 153 is discussed in col. 2, lines 51 – 56)), **and through the contact window of the circumferential electrode to electrically contact the first electrically conductive layer** (e.g. figure 2 shows layer 178 in the contact window of the circumferential electrode that is electrically in contact to the first electrically conductive layer 152 via the conductive layer 154. Conductive layer 154 is discussed in col. 1, line 57), and

i) **connecting the center electrode to input circuit paths to be protected from electrostatic discharge** (e.g. line 3 discloses that center electrode 170 is connected to ground. Electrons travel from negative (ground) to positive, so that the input of the signal is from ground (negative)) **and connecting the circumferential electrode to an electrostatic discharge path comprising either a connection to a circuit ground or a circuit supply voltage** (e.g. figure 2 shows the circumferential electrode 178 connected to the circuit, which necessarily must contain either a circuit supply or circuit ground for current to flow).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Momodomi in view of Chen et al. (US 5,656,534). **Momodomi discloses the integrated circuit chip of claim 1, as cited above, but is silent with respect to the first electrically conductive material being made of polysilicon.**

Chen teaches that an electrically conductive layer forming a polysilicon electrode may be used in electrostatic discharge (ESD) devices (col. 2, line 41, and col. 3, lines 38 – 40, and layer 34 of ESD device shown in figure 1).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to form the integrated circuit chip of Momodomi such that the center electrode is made of polysilicon, as disclosed in Chen for ESD devices. One would be motivated to make an electrode of polysilicon since its properties are well-known in the art and reliable, as discussed by Chen (Background of Invention).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Momodomi in view of Igel et al. (US 6,204,549 B1). **Momodomi discloses the integrated circuit chip of claim 1, as cited above, but is silent with respect to the spark gap cavity containing a noble gas for reducing the breakdown voltage of the electrostatic discharge protection device.**

Igel teaches that a cavity filled with a noble gas may be used in voltage protection devices (col. 2, lines 38 – 40).

It would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the spark gap cavity of Momodomi such that it is filled with a noble gas, since Igel teaches that noble gas filled cavities can be used in between electrodes in protection devices. One would be motivated to make such a modification since a noble gas filled cavity allows one to control the breakdown voltage between the electrodes, as discussed by Igel (col. 2, lines 44 – 47), as well as not being reactive with the electrodes so that there is no corrosive effects.

Response to Arguments

9. Applicant's arguments filed on June 11, 2008 have been fully considered but they are not persuasive. At present, the prior art of Momodomi and El-Kareh remains commensurate to the scope of the claims as stated by the Applicant within the context of the claim language and as broadly interpreted by the Examiner [MPEP 2111], which is elucidated and expounded upon above.

a. With respect to the Applicants argument that Momodomi does not disclose a toroidal spark gap cavity between a circumferential electrode and center electrode, the Examiner respectfully disagrees. As shown in figure 2B of Momodomi, and further clarified in the figure above with respect to claim 1, there is a cavity that is formed between the circumferential electrode 18 and center electrode 17, in which the base layer 13 boarders on the bottom and the cover layer 20 boarders on the top through the protrusion extending downwards. The Applicant agues that this does not form a cavity since there is a material formed

in the cavity, however the formation of the surrounding structures (i.e. the electrodes, base layer, and cover layer) does form an cavity, despite whether or not the cavity is filled with a material.

b. With respect to the Applicant's argument that Momodomi does not disclose a base layer formed by the insulating layer of the integrated circuit chip, the examiner maintains that layer 13 may be considered as an insulating layer, although it is doped with impurities (as implied by the n+ designation). A common definition of "insulating material" is one that "reduces or prevents the transmission of heat or sound or electricity" (e.g. see attached .pdf file), and a common definition of the verb "insulate" is "to separate with a material that reduces the passage, transfer, or leakage of heat, electricity, or sound" (e.g. see attached .pdf file). As seen in figure 2b, the layer 13 has an equivalent resistance R, therefore it reduces the transmission of electricity. Furthermore, the claimed limitation of "an insulating layer of insulating material" does not require an "electrically insulating material" or a specific type of electrical insulating material. One may consider an "insulating layer" to reduce the passage of heat or sound, as noted in the definition of "insulate". The Examiner notes that layer 13 may reduce both the passage of heat and sound through the device. Therefore, the Examiner maintains the layer 13 of Momodomi may be considered an "insulating layer".

Furthermore, Nakane et al (JP 63-223582) discloses that impurity concentrations in semiconductor substrates may have an insulating property at low temperature (abstract). It is also well-known in the art that semiconductors may become insulating at low temperatures due to "carrier freeze out", in which the carriers no longer have enough energy to remain in the conduction energy band. Hence, semiconductor layers may be considered to be insulating layers at certain temperatures.

c. With respect to the Applicant's argument that Momodomi does not disclose a cover layer formed by a dielectric layer of the integrated circuit chip, the Examiner maintains that figure 2B clearly shows layer 20 covering the spark gap cavity, as defined above with respect to claim 1, via the protrusion of layer 20 downward from the remaining layer, wherein the protrusion is directly above the spark gap cavity.

d. With respect to the Applicant's argument that El-Kareh does not disclose depositing a first electrically conductive material on an insulating layer, and depositing a layer of dielectric material on the first electrically conductive layer, the Examiner maintains the El-Kareh clearly discloses depositing a first electrically conductive layer of a first electrically conductive material on said insulating layer (polysilicon layer 152, col. 1, line 56), and depositing a dielectric layer of a dielectric material on said first electrically conductive layer (dielectric

layer 156 of silicon nitride, col. 1, line 58). The Applicant argues that since there is an intervening layer 154 between the first electrically conductive layer 152 and the dielectric layer 156, that the dielectric layer 156 is *not on* the first electrically conductive layer. The examiner respectfully disagrees with the Applicant, since the definition of the word "*on*" may include many relationships, including indication of proximity, place, and location, and that "*on*" does not imply "*direct contact*". Therefore, the dielectric layer 156 may be considered to be *on* the electrically conductive layer 152 of El-Kareh.

e. With respect to Applicant's argument that El-Kareh does not disclose the circumferential electrode, the Examiner maintains that a circumferential electrode 271 is formed in the window 211 formed in figure 1D. In regards to the term "circumferential", a standard definition of circumferential is "lying on the outskirts" (see the attached .pdf). As seen in figure 1E, the electrode 271 may be considered to be "lying on the outskirts" in relation to the left side of the device, and therefore may be considered to be "circumferential".

Another standard definition of "circumferential" is "lying within the circumference". As seen in figure 1E, the electrode 217 is within the circumference of the device, and therefore may be considered to be a "circumferential electrode"

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT HUBER whose telephone number is (571)270-3899. The examiner can normally be reached on Monday - Thursday (9am - 6pm EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892

/Robert Huber/
Examiner, Art Unit 2892
September 3, 2008